

```
graph TD; 102[Central Processing Unit 102] --- 104[Micro code 104]; 104 --- 110[Control Register 110]; 110 --- 112[Request Queue 112]; 110 --- 108[Block Next Request State Machine 108]; 112 --- 114[Request State Machine 114]; 108 --- 106[Bus Controller 106]; 108 --- 116[Arbitration Component 116];
```

The diagram illustrates the control logic of the system. It features a central processing unit (102) which is connected to a micro code component (104). The micro code (104) is connected to a control register (110). The control register (110) is connected to a request queue (112) and a block next request state machine (108). The request queue (112) is connected to a request state machine (114). The block next request state machine (108) is connected to a bus controller (106) and an arbitration component (116).

Figure 1

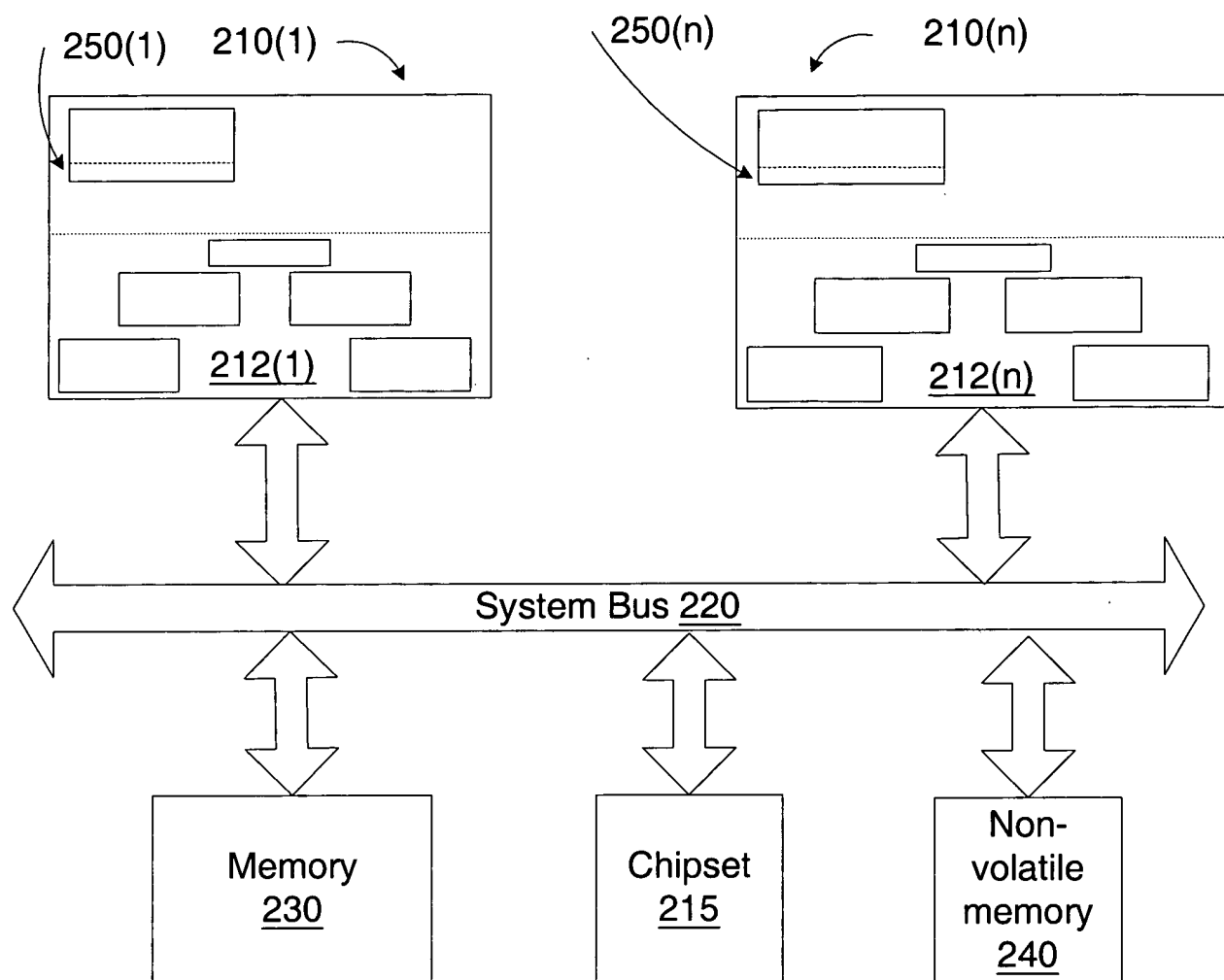


Figure 2

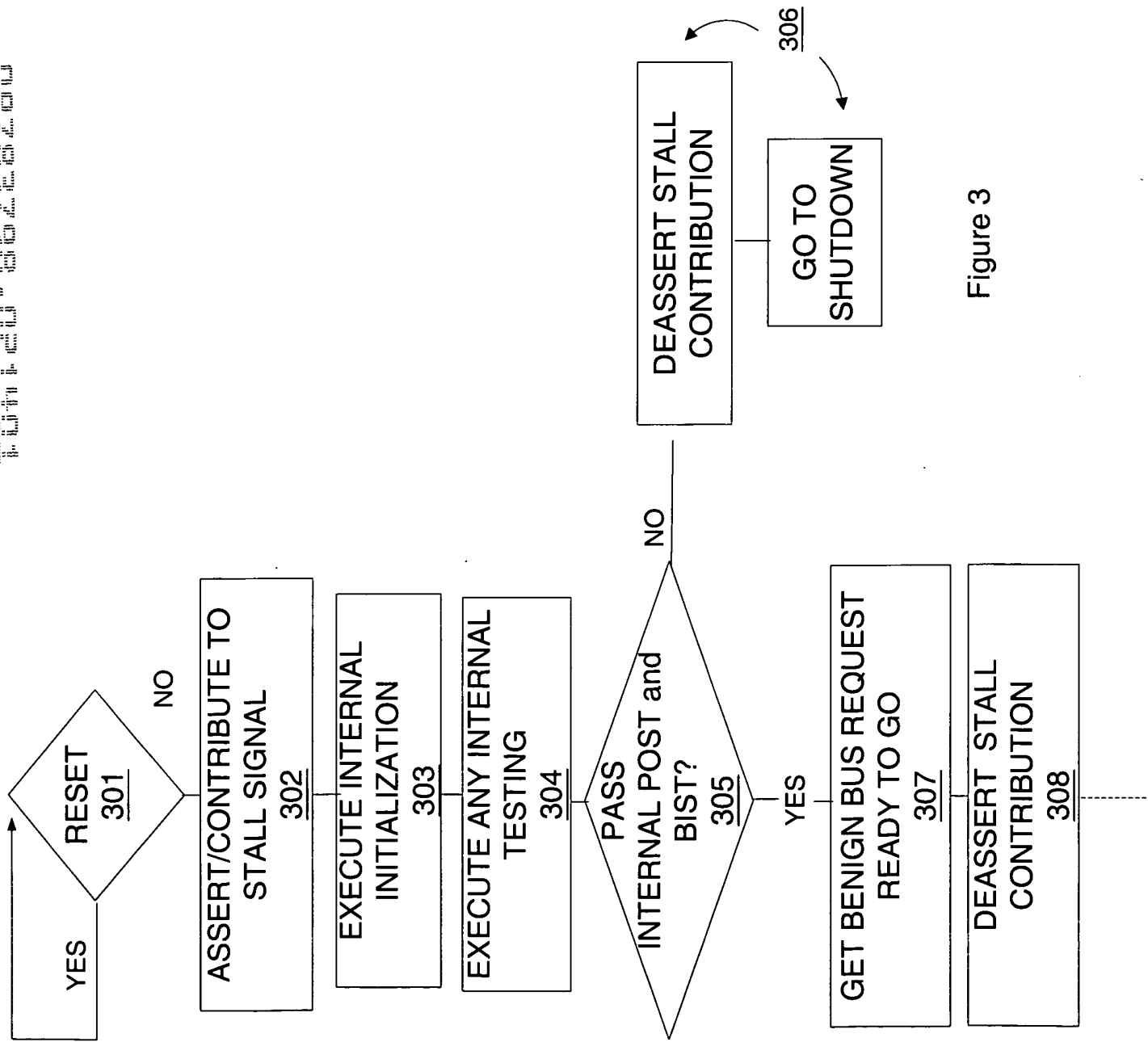


Figure 3

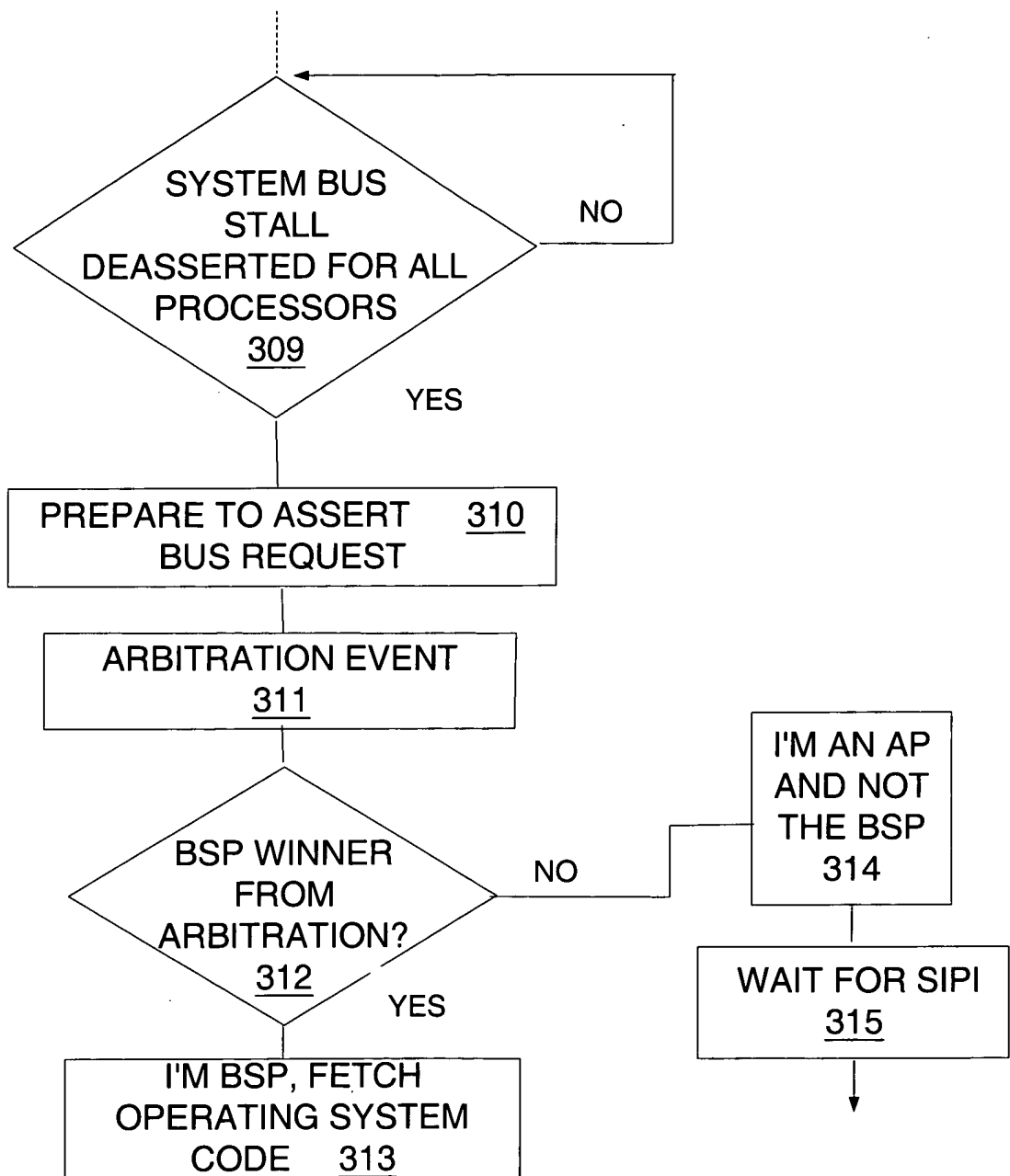


Figure 4